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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,732	11/25/2003	Sheng-Lyang Jang	7257/71612	9806

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EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,732	JANG ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 6, 8, 11* is/are rejected.

7)☒ Claim(s) *7,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A reason for that is that the claim recites following: "a second anode of the SCR is formed by a base of the NPN transistor connected to the negative power supply terminal through a resistor Rx". The term negative power supply is confusing because the NPN transistor emitter becomes an anode only when the backward stress voltage is applied. In such conditions the negative power supply terminal is not negative any more. Additionally, the resistor Rx is not shown in any Drawings, instead resistor Rsub is indicated. For purpose of examination it was interpreted as follows: "a second anode of the SCR is formed by a base of the NPN transistor connected to the grounded power supply terminal through a resistor Rsub".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Metz (US 5,400,202) in view of Miller (US 5,946,177). Regarding Claim 1, Metz

discloses all the elements including a silicon-controlled switch (element 10 in Fig. 4(a)), triggered by MOSFET (element 18 in Fig. 3(a)), which is connected to an emitter of the transistor (element 14 in Fig. 4(a)) and causing the silicon controlled switch to be triggered into conduction. It further discloses a switch control circuit, i.e. transistor control circuit (elements C and R in Fig. 4(a)), installed between the PAD terminal and the gate of the MOSFET (element 25 in Fig. 1). When the forward over-voltage stress occurs over the PAD terminal, the transistor control circuit (elements C and R in Fig. 4(a)), is enabled to turn on the MOSFET (element 18 in Fig. 4(a)) and at the same time the switch control circuit is enabled to trigger the silicon controlled switch (element SCR 10 in Fig. 4(a)) into conduction to form a discharging path, such that the PAD terminal voltage will be rapidly decreased to the level of a holding voltage of the silicon controlled switch to provide ESD protection and prevent latch-up of the silicon controlled switch. It discloses protection of the PAD terminal, which in particular case may be the power supply terminal. However, it does not explicitly disclose protection of the power supply terminal. Miller discloses the ESD protection circuit for the power supply terminal (element 105 in Fig. 3). The circuit uses the same RC triggering schematic (element 125 in Fig. 3) for protection of the power supply terminal (element 105 in Fig. 3) against ESD events. Both references have the same problem solving area, namely providing ESD protection for semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Metz solution by using the circuit for protection against ESD events on the power supply terminals, because (i) as is seen from comparison of Metz and Miller solutions, the

triggering circuits are the same and principle of protection are similar (both circuits use crowbar shunting solutions) and (ii) applying the Metz solution for protection against ESD events on the power supply terminals will help the manufacturer to expand its scope of marketing.

Regarding Claims 2 and 11, Metz discloses the silicon controlled switch formed by an NPN transistor and a PNP transistor (elements 12 and 14 in Fig. 4(a)). It further discloses what Applicant identifies as a first anode of the SCR formed by an emitter of the PNP transistor, and a second anode of the SCR is formed by a base of the PNP transistor which is connected to the positive power supply terminal through a resistor Rn (the Rw resistor in Fig. 4(a)), and a cathode formed by a collector of the PNP transistor which is connected to a base of the NPN transistor and further through a resistor Rsub (element Rs in Fig. 4(a)) to the ground terminal and a gate formed by the base of the PNP transistor connected to a collector of the NPN transistor. Please, note that the first and second anodes are electrically identical.

As per Claim 11, it differs from Claim 2 rejected above by is functional limitation of behavior of the silicon controlled rectifier subjected to backward overvoltage stress. When the Metz circuit is being subjected to the backward overvoltage stress, it would behave the same way as claimed circuit, i.e. it would provide discharging path through base-collector junction of the NPN transistor (element 14 in Fig. 4(a)) to the positive supply terminal. Therefore, Metz discloses the silicon controlled switch formed by an NPN transistor and a PNP transistor (elements 12 and 14 in Fig. 4(a)), what Applicant calls a first anode of the SCR formed by an emitter of the NPN transistor, and a second

anode of the SCR is formed by a base of the NPN transistor connected to the negative power supply terminal through a resistor sub (resistor Rs in Fig. 4(a)), and a cathode formed by a collector of the NPN transistor which is connected to a base of the PNP transistor, and a gate of the SCR is formed by the base of the NPN transistor which is connected to a collector of the PNP transistor.

Regarding Claim 3, Metz discloses the transistor control circuit formed by a capacitor and a resistor (elements C and R in Fig. 4(a)), and the capacitor-resistor node is connected to the gate of the metal oxide semiconductor field effect transistor (element 18 in Fig. 4(a)), such that a time constant of the circuit can be determined by adjusting the values of the capacitor and the resistor, so as to control the conduction time of the MOSFET (col. 6, line 59 – col. 7, line 9).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Metz in view of Miller et al. and Applicant Admitted Prior Art (AAPA). Metz and Miller et al. disclose all the elements of Claims 1 and 2. However, regarding Claim 4, they do not disclose a Zener diode. AAPA discloses the switch control circuit having a Zener diode (element ZD in Fig. 11) connected across the base electrodes of complementary PNP/NPN transistors in the silicon controlled switch, so that a discharge current can continue after the MOSFET is disabled. When the supply voltage is sufficient for breakdown of the Zener diode, the diode will conduct, thus forcing both transistor into conduction and due to a positive feedback, to saturation. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have

further modified the Metz solution by adding the Zener diode according to AAPA, because as AAPA states (page 4, lines 5 – 10), this solution has advantage of lower triggering voltage.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Metz in view of Miller et al., Applicant Admitted Prior Art (AAPA) and Wodarczyk et al. (US 5,079,608). Metz, Miller et al. and AAPA disclose all the elements of Claims 1, 2 and 4. However, regarding Claim 5, they do not disclose the Zener diode connected in series by a diode. Wodarczyk et al. disclose the Zener diode (element D4 in Fig. 1) of the switch control circuit connected in series by a diode (element D3 in Fig. 1). Both references have the same problem solving area, namely providing an overvoltage protection to the semiconductor devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Metz solution by adding the diode in series with the Zener diode of AAPA, because as Wodarczyk et al. state (col. 3, lines 4 – 10), the diode protects the Zener diode against reverse polarity voltages.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Metz in view of Miller and Piccone et al. (US 3,886,432). As was stated above, Metz and Miller disclose all the elements of Claims 1 and 2. However, regarding Claim 6, they do not disclose the silicon controlled switch connected to the ground terminal through a diode array in series. Piccone et al. disclose the silicon controlled switch (elements 27 in Fig.

2) connected to the ground terminal through a diode array (elements 28 in Fig. 2) in series. Both references have the same problem solving area, namely overvoltage protection for semiconductor elements. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Metz solution by adding the diode array connected in series with the silicon controlled switch according to Piccone et al., because as Piccone et al. state (col. 4, lines 40 – 45), the diodes ensure that the circuit has a reverse blocking means capable of withstanding high voltage.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Metz in view of Miller and Piccone et al. and Court Decision *In re Japikse,* 181 F.2d 1019, 86 USPQ 70 (CCPA 1950). Claim 8 differs from Claim 8 rejected above by its diode array position; it is positioned in series with the power supply terminal rather than in series with the ground terminal. The Court Decision addresses this issue stating that rearranging parts of an invention involves only routine skill in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Metz solution in view of Piccone et al. solution of by placing the diode array in series with the power supply rather than in series with the ground terminal, since it has been held that rearranging parts of the invention involves only routine skill in the art.

Allowable Subject Matter

Claims 7, 9, 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is that Claims 7 and 9 recite limitations of MOSFET connected between either positive power supply, or negative power supply and the silicon controlled switch. Such limitation was not found in a collected prior art of the record. As per Claim 10, it recites limitation of the NMOS connected across the base electrodes of the complementary PNP/NPN transistors. Such limitation was not found in a collected prior art of the record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
02/18/2005

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